ABSTRACT

Methods for forming a gate in a semiconductor device are disclosed. In an example method, the gate is formed such that the CD of an upper portion of the gate is greater than the CD of a lower portion of the gate by performing multiple etching processes. In an illustrated example, the etching processes are performed in three stages, (i.e., a first dry etching process for etching the upper portion, a second dry etching process for etching the lower portion and a third dry etching) under three different process conditions, thereby causing a sidewall profile of the gate to have a two-layered structure.